REMARKS

This is in response to the Office Action dated March 15, 2005. Claims 16-23 are pending.

General

For purposes of example, and without limitation, certain example embodiments of this invention relate to a semiconductor device having a structure which allows for easier processing and alignment during the manufacture thereof. For example, Fig. 1 of the instant application illustrate a semiconductor device including *metal* gate electrode 19, gate insulator 13, respective *metal* contact plugs 20 provided over S/D regions 15, and interlayer insulator 22 provided over both the gate electrode 19 and isolation regions 12 (e.g., see especially Figs. 1(f) – 1(j)). *The metal gate electrode 19 directly contacts an upper surface of the gate insulating film 13 so that only the gate insulating film 13 is located between the metal gate electrode 19 and a channel of a transistor for which the gate electrode is provided.* The gate electrode 19 is electrically isolated from the contact plugs 20 by the sidewall insulating film(s) 16, and the gate electrode 19 and the contact plugs 20 both have the same height as best shown in Fig. 1(i). Since the gate electrode 19 and contact plugs 20 are both formed of metal, they advantageously may both be formed in the same process step using the same material. This unique structure is advantageous in that it allows an easier process of manufacture as explained above and also permits contact plugs 20 to be formed in the vicinity of the gate electrode 19 in a self-aligned manner, so that electrical isolation between the gate electrode 19 and contact plugs 20 is ensured for prevention of a short between the gate electrode and the contacts of the interconnection (e.g., pgs. 24-25). Further, the contact plugs 20 can be spaced by a minimum distance from the gate electrode 19 as desired by adjusting the thickness of the sidewall insulating film 16. Therefore, the contacts can be

provided close to the gate electrode, whereby a parasitic resistance in the source/drain regions can be reduced for improvement of the device characteristics of the transistor (e.g., pg. 25).

Art Rejection

The previous ground of rejection has been withdrawn. However, a new ground of rejection has been made. This new rejection is incorrect for at least the following reasons.

Claim 16 stands rejected under 35 U.S.C. Section 103(a) as being allegedly unpatentable over Fuller in view of Buynoski. This Section 103(a) rejection is respectfully traversed for at least the following reasons.

Claim 16 requires "a metal gate electrode provided on a semiconductor substrate with the intervention of a gate insulating film, wherein the metal gate electrode directly contacts an upper surface of the gate insulating film so that only the gate insulating film is located between the metal gate electrode and a channel of a transistor for which the gate electrode is provided; a sidewall insulating film provided on a side wall of the metal gate electrode; source/drain regions provided in the semiconductor substrate for the transistor, the channel being provided between the source/drain regions; metal contact plugs provided on the source/drain regions; wherein the metal gate electrode is electrically isolated from the metal contact plugs by the sidewall insulating film alone; wherein the metal gate electrode is partly or entirely composed of the same material as the metal contact plugs; wherein the metal gate electrode and the metal contact plugs have the same height." For purposes of example only, Fig. 1 illustrates that the metal gate electrode 19 directly contacts an upper surface of the gate insulating film 13 so that only the gate insulating film 13 is located between the metal gate electrode 19 and a channel of a transistor for which the gate electrode is provided. Moreover, the metal gate electrode 19 is partly or entirely composed of the same material as the metal contact plugs 20 which are isolated from the gate

electrode via insulator(s) 16; and the metal gate electrode 19 and the metal contact plugs 20 have the same height.

Fuller fails to disclose or suggest the aforesaid quoted and underlined features of claim 16. In particular, Fuller in Figs. 2E-2F discloses polysilicon gate electrode 211, source/drain regions 213/214,gate insulator 215, and insulating gate sidewall spacers 221. As shown in Figs. 2D-2E of Fuller, a tungsten layer 223 is deposited over the gate and source/drain regions of the transistor and is thereafter planarized so that tungsten portion 231 is provided over the gate and tungsten portions 232, 233 are provided over the source/drain regions (e.g., col. 4, lines 20-55). However, in contrast with Fuller, claim 16 requires that "*the metal gate electrode directly contacts an upper surface of the gate insulating film so that only the gate insulating film is located between the metal gate electrode and a channel of a transistor.*" Fuller fails to disclose or suggest these features of claim 16 in view of Fuller's requirement for polysilicon (non-metal) gate electrode 211. Fuller teaches directly away from the invention of claim 16 by requiring non-metal gate electrode 211. Moreover, because of Fuller's use of a non-metal gate electrode, Fuller's structure is highly undesirable because it requires an additional non-metal layer 211 in between the gate insulator 215 and metal 231 thereby adding significant costs and processing requirements to the overall device. In other words, Fuller cannot possibly form the gate electrode 211 and the alleged plugs 232, 233 all in the same step because they are of much different materials – Fuller is highly undesirable in this regard.

Apparently recognizing the above-listed deficiencies in Fuller, the Office Action has cited new art to Buynoski. Buynoski in Fig. 16 appears to disclose a metal gate electrode 128b directly contacting an underlying gate insulator. The Office Action contends that it would have

been obvious to have provided Fuller with a metal gate electrode that directly contacts the gate insulator as in Buynoski.

However, this Section 103(a) modification/combination is incorrect for at least the following reasons. Fuller requires polysilicon portion 211 in order to (a) implant impurities into the channel (col. 3, lines 49-51), (b) implant impurities to form the source/drain regions using the polysilicon as a mask (col. 3, lines 66-67), and (c) form the sidewall spacers. Thus, the use of polysilicon portion 211 is required in Fuller's process and device. One of ordinary skill in the art would never have removed it as alleged in the Section 103(a) rejection because the above-listed steps then could not properly be performed. Thus, one of ordinary skill in the art would not have removed 211 as alleged in the Office Action because this would destroy the functionality and purpose of the base reference.

For at least the foregoing reasons, it is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance. If any minor matter remains to be resolved, the Examiner is invited to telephone the undersigned with regard to the same.

Respectfully submitted,

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